4-bit Multiplexer/Demultiplexer Chip Set for 40-Gbit/s Optical Communication Systems

Kiyoshi Ishii, Hideyuki Nosaka, *Member, IEEE*, Minoru Ida, *Member, IEEE*, Kenji Kurishima, Shoji Yamahata, Takatomo Enoki, *Senior Member, IEEE*, Tsugumichi Shibata, *Senior Member, IEEE*, and Eiichi Sano, *Member, IEEE*

***Abstract*—We have designed and fabricated a low-power 4 : 1 multiplexer (MUX), 1 : 4 demultiplexer (DEMUX) and full-clock-rate 1 : 4 DEMUX with a clock and data recovery (CDR) circuit using undoped-emitter InP–InGaAs HBTs. Our HBTs exhibit an f_T of approximately 150 GHz and an $f_{\max}$ of approximately 200 GHz at a collector current density of 50 kAμm^2. In the circuit design, we utilize emitter-coupled logic and current-mode logic series gate flip-flops and optimized the collector current density of each transistor to achieve low-power operation at required high bit rates. Error-free operation at bit rates of up to 50 Gbit/s were confirmed for the 4 : 1 MUX and 1 : 4 DEMUX, which dissipates 2.3 and 2.5 W, respectively. In addition, the full-clock-rate 1 : 4 DEMUX with the CDR achieved 40-Gbit/s error-free operation.**

***Index Terms*—Clock and data recovery (CDR), demultiplexer (DEMUX), HBT, InP, integrated-circuit (IC) design, multiplexer (MUX), optical communications.**

I. Introduction

THERE ARE strong demands for more transmission capacity in optical communications systems to support various communication services. High-speed integrated circuits (ICs) are necessary for broad-band optical communications systems. A multiplexer (MUX), a demultiplexer (DEMUX), and a clock and data recovery (CDR) circuit are key components of these systems and measuring equipment. Considerable work related to the design and fabrication of over-40-Gbit/s-class MUX, DEMUX, and CDR circuits has been carried out using InP-based HBTs [1]–[4], SiGe-based HBTs [5]–[9], and InP-based high electron-mobility transistors (HEMTs) [10], [11].

InP-based HBTs offer high internal gain and excellent high-frequency performance. In addition, we have developed undoped-emitter InP–InGaAs HBT technology [12], [13]. The undoped-emitter structure offers higher cutoff frequency f_T than the conventional n-doped-emitter one at low collector current density. Thus, undoped-emitter InP–InGaAs HBTs are potentially attractive for high-speed high-sensitivity ICs with low-power consumption. In this study, we employed undoped-emitter InP–InGaAs HBT technology to fabricate a 4 : 1 MUX, 1 : 4 DEMUX, and a full-clock-rate 1 : 4 DEMUX with a CDR circuit for over-40-Gbit/s optical communications systems and measuring equipment.

Manuscript received April 17, 2003; revised June 27, 2003.

K. Ishii, H. Nosaka, M. Ida, K. Kurishima, S. Yamahata, T. Enoki, and T. Shibata are with NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan (e-mail: ishii@aecl.ntt.co.jp).

E. Sano was with NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan. He is now with the Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo 060-8628, Japan.

Digital Object Identifier 10.1109/TMTT.2003.818582

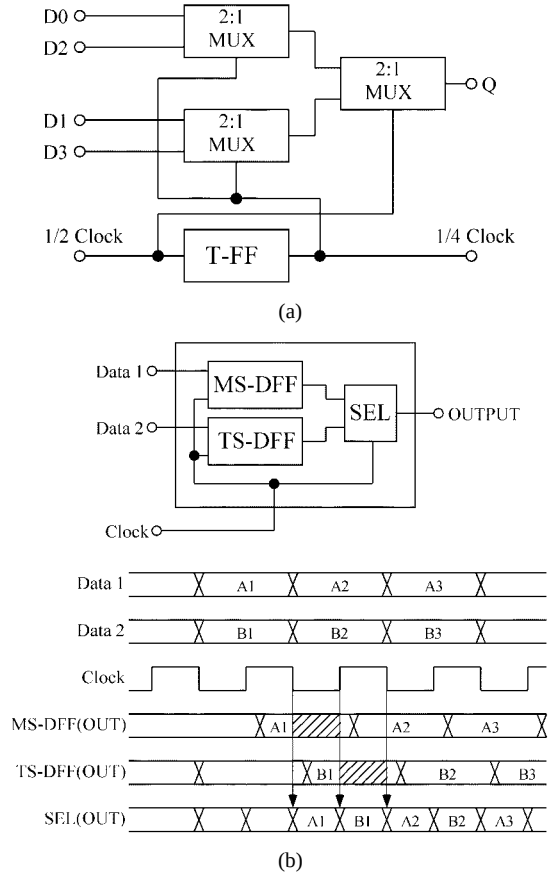


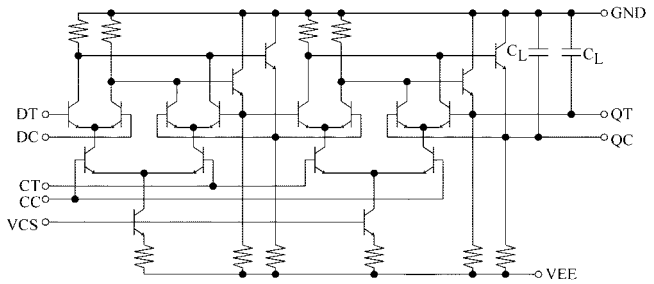
Fig. 1. 4 : 1 MUX IC. (a) 4 : 1 MUX architecture. (b) 2 : 1 MUX block and the timing chart.

In this paper, we present the circuit design and experimental results for the 4-bit MUX/DEMUX chip set. Section II discusses the circuit design of the 4 : 1 MUX, 1 : 4 DEMUX, and CDR circuit for achieving high-bit-rate operation with low-power consumption. Section III briefly describes our InP–InGaAs HBT technology. Section IV presents the measuring systems and measured IC performances.

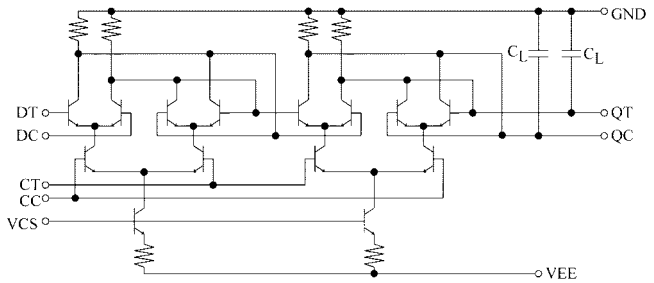
II. Circuit Design

A. 4 : 1 MUX

Fig. 1 is a schematic of the 4 : 1 MUX. We adopt the conventional tree-type architecture. The 2 : 1 MUX block consists of a three-stage D flip-flop (TS-DFF), master–slave D flip-flop (MS-DFF), and selector (SEL) gate to get a wide phase margin, as shown in the timing chart. By using the TS-DFF, the data-2 signal is delayed by a half bit from the data-1 signal. The half-bit



(a)



(b)

Fig. 2. Circuit configurations of the master–slave flip-flop. (a) ECL type. (b) CML type.

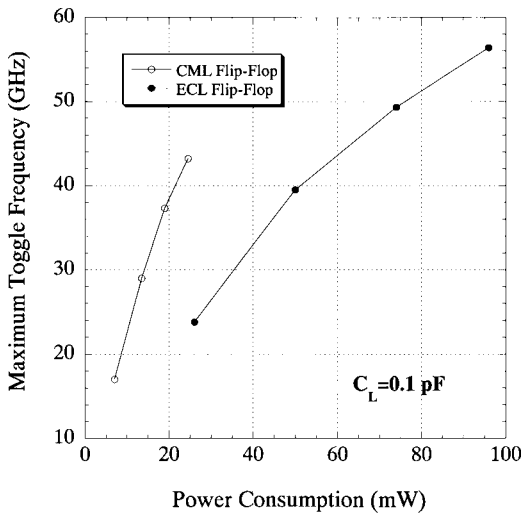


Fig. 3. Simulated power consumption dependence of maximum toggle frequencies.

delay ensures a wide phase margin for selecting the data signals in the SEL gate.

An emitter-coupled logic (ECL) and a current-mode logic (CML) series gate are used for the flip-flops and the SEL gate. The circuit configurations of the MS-DFF are shown in Fig. 2. In this paper, the flip-flop consisting of current switches and emitter followers is called the ECL flip-flop [see Fig. 2(a)]. The flip-flop consisting of current switches only is called the CML flip-flop [see Fig. 2(b)]. Fig. 3 shows the simulated power consumption dependence of the maximum toggle frequency for both flip-flops, where C_L is the load capacitance, which includes the loading effects of subsequent devices and the capacitance of the interconnecting metal layer. We roughly assume that C_L is 0.1 pF. The device parameters of our InP–InGaAs HBT were used for the SPICE simulation. The ECL flip-flop has the emitter follower between the master latch and slave one. The input impedance of the emitter follower is very high and the output impedance is very low. This results in high-speed switching of upper-level current switch transistors. In addition, by using the emitter follower, the upper-level current switch transistors are appropriately biased between the base and collector to minimize the base–collector capacitance C_{BC}. On the other hand, the upper-level current switch transistors of the CML flip-flop were biased in the soft saturation region. Therefore, the maximum toggle frequency of the ECL flip-flop is much higher than the CML one. The ECL flip-flop is attractive for high-speed operation. Therefore, we used the ECL flip-flop in the final 2 : 1 MUX stage. Over-50-GHz flip-flop operation is expected using our InP–InGaAs HBTs.

On the other hand, the CML flip-flop is attractive for low-power operation at operating speeds below 40 GHz. For example, to achieve 30-GHz operation, the ECL and the CML flip-flops consume approximately 35 mW/flip-flop and 15 mW/flip-flop, respectively, as shown in Fig. 3. The power consumption of the CML flip-flop is below half that of the ECL one. In order to achieve accurate operation with low-power consumption, we adopted the CML flip-flop in the 4 : 2 MUX stages. The collector current densities (J_C's) of the HBTs in the CML flip-flop were designed to be about half that of the ECL flip-flop to reduce the power consumption as much as possible. The internal voltage swing is designed to be 0.5 V for both flip-flops.

Other key blocks to achieve both high-speed operation and low-power consumption are the clock distribution circuits, which are shown in Fig. 4. The high current density of current switch transistors results in high-speed switching. The J's of current switch transistors were optimized for the required operating speed. For the emitter follower transistors in Fig. 4(a) and the second emitter follower ones in Fig. 4(b), there is a tradeoff between the driving capability and power consumption. Therefore, we optimized the number of transistor and J's of the transistors on the emitter followers by determining the required operating speed and number of fan-outs. In optimizing, we also took the parasitic resistance and capacitance of interconnecting metal layers into consideration. The parasitics were extracted from the layout patterns and back-annotated in the design cycle.

B. 1 : 4 DEMUX

A block diagram of the 1 : 4 DEMUX is shown in Fig. 5. The 1 : 4 DEMUX employs the conventional tree-type architecture. The 1 : 2 DEMUX consists of a TS-DFF and MS-DFF. As shown in the timing chart, a wide phase margin is obtained by using the TS-DFF. The 1 : 2 DEMUX and the 2 : 4 DEMUX stages use flip-flops based on ECL and CML series gates, respectively. The J_C's of each transistor for the clock distribution circuits in the 1 : 4 DEMUX are also optimized. The principle of circuit design is much the same as the 4 : 1 MUX.

C. 1 : 4 DEMUX With CDR

The one-chip full-clock-rate 1 : 4 DEMUX with CDR monolithically integrates a linear-type phase detector (PD), a lag-lead low-pass filter (LPF), full-rate voltage-controlled oscillator (VCO), 1 : 4 DEMUX, and toggle flip-flop (T-FF), as

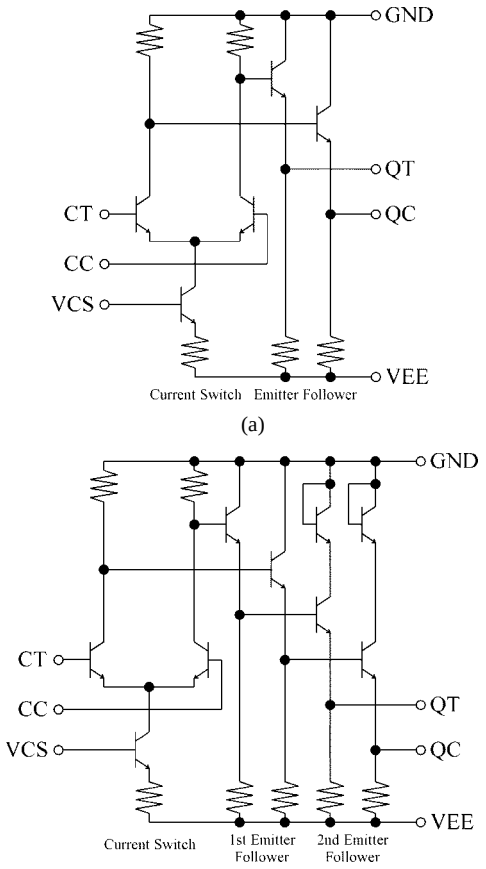


Fig. 4. Circuit configurations of the clock distribution circuits. (a) Second-level output. (b) Third-level output.

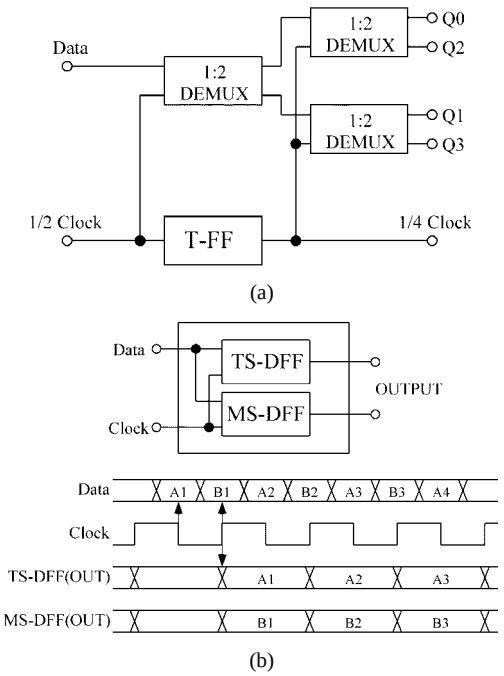


Fig. 5. 1 : 4 DEMUX IC. (a) 1 : 4 DEMUX architecture. (b) 1 : 2 DEMUX block and the timing chart.

shown in Fig. 6. The 1 : 4 DEMUX mentioned in Section II-B is used as the DEMUX in this IC. The linear-type PD enables low-power operation because it can be constructed with few

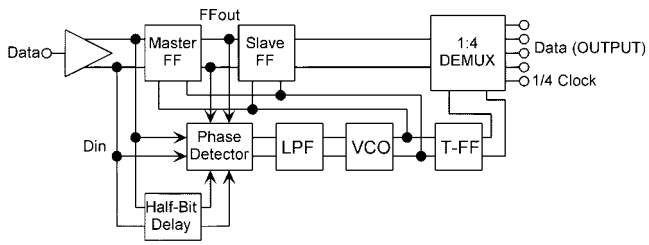


Fig. 6. One-chip full-clock-rate 1 : 4 DEMUX with the CDR.

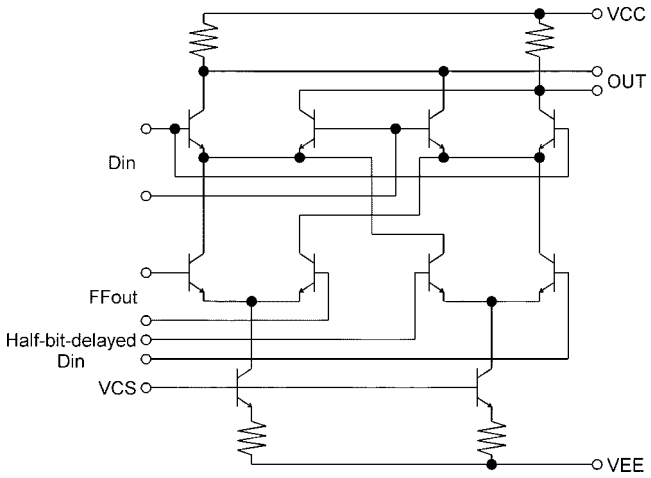


Fig. 7. Circuit configuration of the PD.

transistors compared with other types of PDs. It offers a wide pull-in range without a frequency acquisition circuit.

The half-bit-delayed data is used as standard timing data. The PD outputs a signal pulse that includes phase error by comparing the Din, $FFout$, and the half-bit-delayed data. The phase error signal is filtered by the LPF, which suppresses the high-frequency signal components. The LPF output signal controls the VCO. The VCO outputs a 40-GHz clock signal. This IC was designed to operate at the full clock rate of 40 GHz. The IC consists of 531 transistors and 368 resistors.

The configuration of the PD is shown in Fig. 7. It consists of two multiplier circuits to improve tolerance to data signal mark ratio variations [14] and data transition density variations. One multiplier detects phases between the input data Din and $FFout$ by calculating $Din \times FFout$. The calculated data, however, contains data-transition-density information. The other multiplier detects only the data-transition-density information by calculating $Din \times$ half-bit-delayed Din. The PD roughly compensates the effect of the data transition density on the dc level of the PD output by finding the difference between the two multipliers' outputs.

Photographs of the 4 : 1 MUX, 1 : 4 DEMUX, and full clock rate 1 : 4 DEMUX with the CDR are shown in Fig. 8. The chip size is 3×3 mm^2 for all ICs. The power supply voltage was designed to be -4.5 V.

III. Fabrication Technology

The undoped-emitter InP–InGaAs HBTs used in this study were grown by metalorganic vapor phase epitaxy (MOVPE) on a 3-in semi-insulating InP substrate. Carbon was the base

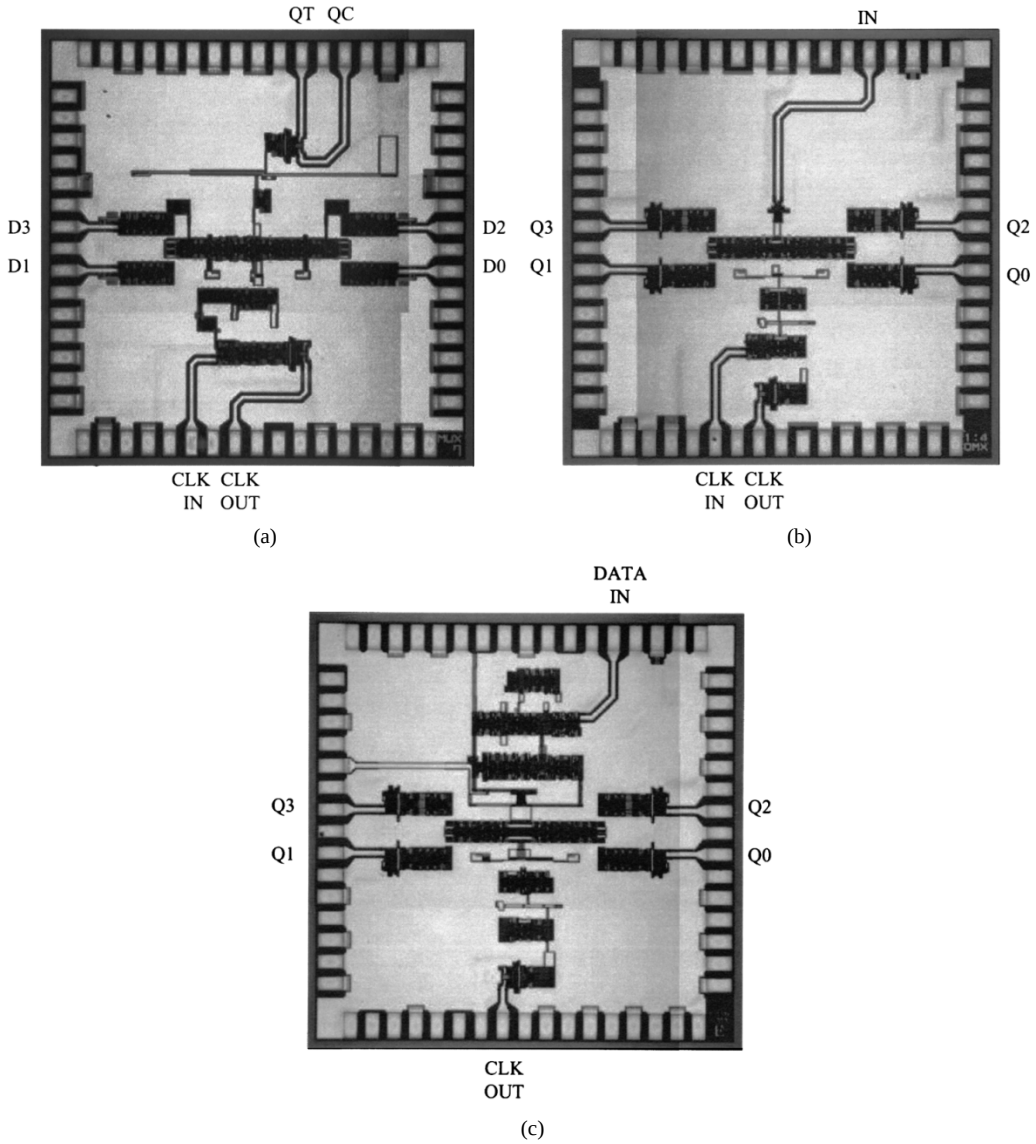


Fig. 8. Photographs of the: (a) 4 : 1 MUX, (b) 1 : 4 DEMUX, and (c) 1 : 4 DEMUX with the CDR.

dopant. We employed a simple nonself-aligned process to make these ICs [12]. The HBT has a 70-nm-thick undoped InP emitter, a 50-nm-thick carbon-doped InGaAs base, and a 300-nm-thick InGaAs collector. The f_T and maximum oscillation frequency $f_{\max}$ were approximately 150 and 200 GHz at a collector current density of 50 kA/cm^2 and a collector-to-emitter voltage of 1.2 V. In this study, all transistors have an emitter width of 1.0 μm.

IV. IC Performance

Measurements of ICs were performed on-wafer using RF probes. Schematic diagrams of the measuring systems are shown in Fig. 9, where (a) is the measuring system for the 4 : 1 MUX and (b) is that for the 1 : 4 DEMUX and the full-clock-rate 1 : 4 DEMUX with the CDR. For measurement of the 4 : 1 MUX, the four input data signals up to 12.5 Gbit/s with word length of $2^{31}-1$ were generated by a four-channel pulse-pattern generator (PPG). The output data signal (QT) of the device-under-test (DUT) were demultiplexed into four-channel data signals using a DEMUX module consisting of GaAs MESFET and InP HEMT ICs [15]. Error-free operation was confirmed at every channel using a four-channel error detector. The output data (QC) and the output clock (CLK/4) signals were monitored with an oscilloscope. We measured the clock phase margins by shifting the four input data signals using phase shifter A.

For measurement of the 1 : 4 DEMUX and 1 : 4 DEMUX with the CDR, we generated a pseudorandom bit stream (PRBS) of up to 50 Gbit/s by quadrupling a PRBS of up to 12.5 Gbit/s with a word length of $2^{31}-1$ using a MUX module. The phase shifter was used to shift the data signal to measure the phase margin. The output data signals of the DUT were connected with the four-channel error detector or the oscilloscope. We also confirmed error-free operation of every channel in this case. The input clock signal of the DUT (CLK/2) was not needed for the measurement of 1 : 4 DEMUX with the CDR.

The 4 : 1 MUX operated a bit error rate of less than 1×10^{-11} at a bit rate of up to 50 Gbit/s. Dead bands were not observed.

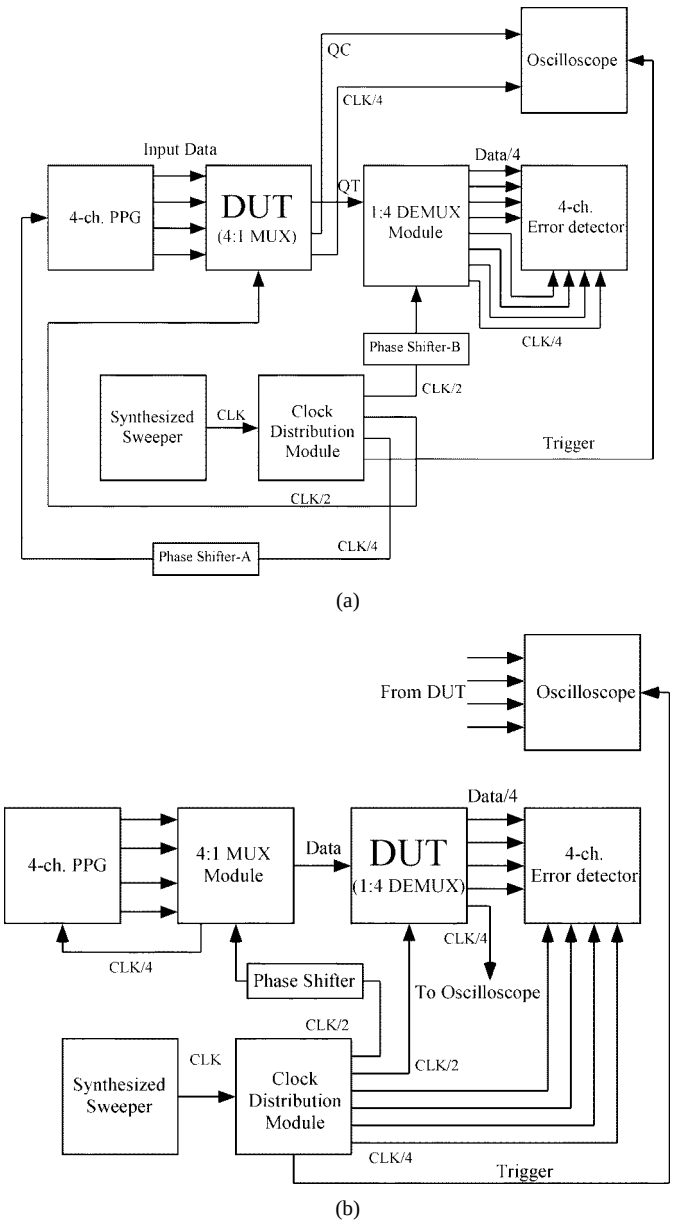


Fig. 9. Schematic diagram of the measuring systems for: (a) 4 : 1 MUX, (b) 1 : 4 DEMUX, and 1 : 4 DEMUX with the CDR circuit.

Both input data and clock signal amplitudes were set at approximately 0.9 Vp-p. The clock phase margins were approximately 200° and 180° at 45 and 50 Gbit/s, respectively. These phase margins include the skew for the four-channel input data signals. The output pattern had a good eye opening at 50 Gbit/s, as shown in Fig. 10. The accumulation time was 15 s. Output data swing was approximately 0.79 Vp-p. The rise and fall times (20%–80%) were approximately 9.6 and 6.7 ps, respectively. The output data peak-to-peak and rms jitters were approximately 5.8 and 1.1 ps, respectively.

The 1 : 4 DEMUX also operated a bit error rate of less than 1×10^{-11} at a bit rate of up to 50 Gbit/s without dead bands. High input sensitivity of below 38 mV (eye height) was obtained at 50 Gbit/s. The clock signal amplitude was set at approximately 0.9 Vp-p. The clock phase margin was approximately 140° at 50 Gbit/s with the data signal amplitude of approximately 0.9 Vp-p. Fig. 11 shows a typical demultiplexed output eye pattern (channel 1) at the input data rate of 50 Gbit/s. Almost the same eye pattern was obtained at the other channels. Output data swing was approximately 0.65 Vp-p. The rise and fall times (20%–80%) were approximately 28 and 23 ps, respectively. The output data peak-to-peak and rms jitter were approximately 15 and 3 ps, respectively. The maximum operating speed of 50 Gbit/s for both 4 : 1 MUX and 1 : 4 DEMUX is not limited by the IC performances, it is limited by the measurement equipment performance. Over-50-Gbit/s operation will be achievable for both ICs.

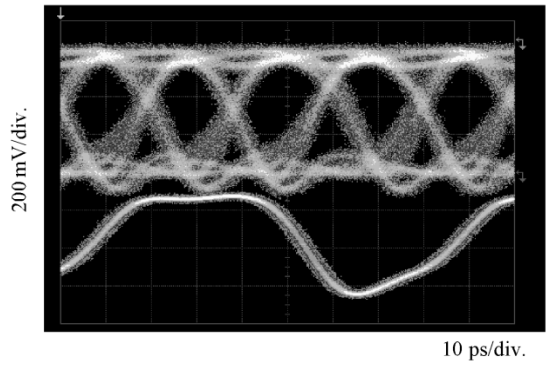


Fig. 10. Output eye pattern of the 4 : 1 MUX at 50 Gbit/s (upper) and output clock signal (lower).

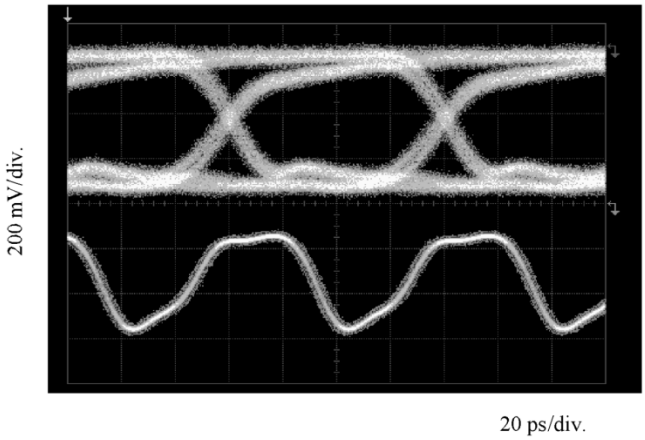


Fig. 11. One of the output eye patterns of the 1 : 4 DEMUX at 50 Gbit/s (upper) and the output clock signal (lower). Almost the same eye pattern was obtained at the other channels.

The full clock rate 1 : 4 DEMUX with the CDR was operated at 40 Gbit/s. The 1/4 clock signal and the demultiplexed output eye patterns are shown in Fig. 12. Good eye opening was obtained. The error-free operation at 40 Gbit/s was confirmed. Fig. 13 shows the measured phase noise of the recovered 1/4 clock signal (10 GHz). The phase noise at 1-MHz off-carrier was −118 dBc/Hz.

Low power consumptions of approximately 2.3, 2.5, and 3.6 W were achieved for the 4 : 1 MUX, 1 : 4 DEMUX, and full-clock-rate 1 : 4 DEMUX with the CDR, respectively. It can also be said based on by our results that a 4 : 1 MUX with a clock multiplier unit (CMU) circuit will be achievable by using the 4 : 1 MUX and the phase-locked loop (PLL) architecture of the CDR circuit in this study.

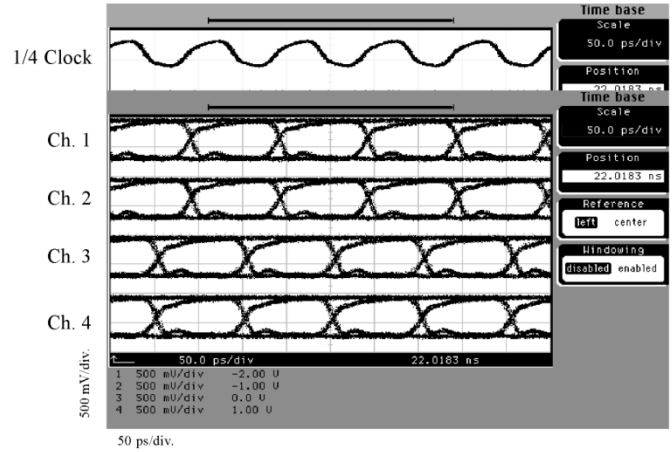


Fig. 12. 1/4 output clock signal (upper) and output eye patterns of the 1 : 4 DEMUX with the CDR at 40 Gbit/s.

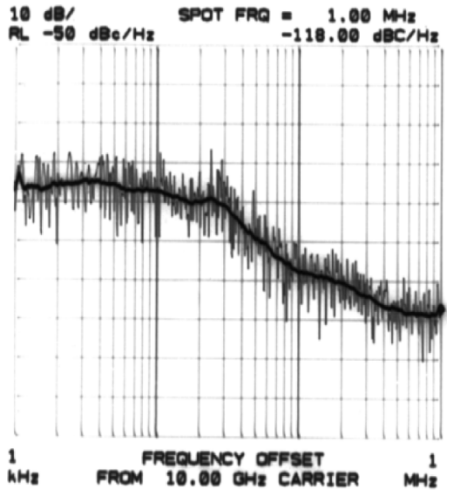


Fig. 13. Measured phase noise of recovered 1/4 clock signal for 1 : 4 DEMUX with the CDR.

V. Conclusion

We have successfully designed and fabricated a low-power 4 : 1 MUX, 1 : 4 DEMUX, and full-clock-rate 1 : 4 DEMUX with a CDR using undoped-emitter InP–InGaAs HBT technology. Up-to-50 Gbit/s error-free operation was confirmed for the 4 : 1 MUX and 1 : 4 DEMUX, respectively, and 40-Gbit/s full-clock-rate operation of the 1 : 4 DEMUX with the CDR was achieved. Low power consumptions of approximately 2.3, 2.5, and 3.6 W were obtained for the 4 : 1 MUX, 1 : 4 DEMUX, and full clock rate 1 : 4 DEMUX with the CDR, respectively. The results of our study demonstrate that undoped-emitter InP–InGaAs HBT technology is an excellent choice for fabricating high-speed low-power ICs for optical communications systems and measuring equipment operating at bit rates of over 40 Gbit/s.

Acknowledgment

The authors thank M. Muraguchi and H. Toba, both of NTT Photonics Laboratories, Kanagawa, Japan, for their encouragement and valuable suggestions. The authors also thank K. Murase, M. Hirata, K. Fujimoto, Y. Takeo, H. Taira, S. Moriyama, N. Tsuji, and S. Kurita, all of the NTT Electronics Corporation, Tokyo, Japan, for their support.

References

[1] J. P. Mattia, R. Pullela, G. Georgieu, Y. Baeyens, H. S. Tsai, Y. K. Chen, C. Dorschky, T. Winkler Von Mohrenfels, M. Reinhold, C. Groepper, M. Sokolich, L. Nguyen, and W. Stanchina, "High-speed multiplexer: A 50 Gb/s 4 : 1 MUX in InP HBT technology," in *GaAs Integrated Circuits Symp. Tech. Dig.*, 1999, pp. 189–192.

[2] J. P. Mattia, R. Pullela, Y. Baeyens, Y.-K. Chan, H.-S. Tsai, G. Georgiou, T. Winkler Von Mohrenfels, M. Reinhold, C. Groepper, C. Dorschky, and C. Schulien, "A 1 : 4 demultiplexer for 40 Gb/s fiber-optic applications," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, 2000, pp. 64–65.

[3] H. Nosaka, E. Sano, K. Ishii, M. Ida, K. Kurishima, T. Enoki, and T. Shibata, "A fully integrated 40-Gbit/s clock and data recovery circuit using InP/InGaAs HBTs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2002, pp. 83–86.

[4] J. Yen, M. G. Case, S. Nielsen, J. E. Rogers, N. K. Srivastava, and R. Thiagarajah, "A fully integrated 43.2 Gb/s clock and data recovery and 1 : 4 DEMUX IC in InP HBT technology," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2003, pp. 240–241.

[5] T. Masuda, K. Ohhata, N. Shiramizu, E. Ohue, K. Oda, R. Hayami, H. Shimamoto, M. Kondo, T. Harada, and K. Washio, "40 Gb/s 4 : 1 multiplexer and 1 : 4 demultiplexer IC module using SiGe HBTs," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2001, pp. 1697–1700.

[6] M. Reinhold, C. Dorschky, R. Pullela, E. Ross, P. Mayer, P. Paschke, Y. Baeyens, J. P. Mattia, and F. Kunz, "A fully-integrated 40 Gb/s clock and data recovery/1 : 4 DEMUX IC in SiGe technology," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2001, pp. 84–85.

[7] M. Meghelli, A. V. Rylyakov, and L. Shan, "50 Gb/s SiGe BiCMOS 4 : 1 multiplexer and 1 : 4 demultiplexer for serial communication systems," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2002, pp. 260–261.

[8] A. Koyama, T. Harada, H. Yamashita, R. Takeyari, N. Shiramizu, K. Ishikawa, M. Ito, S. Suzuki, T. Yamashita, S. Yabuki, H. Ando, T. Aida, K. Watanabe, K. Ohhata, S. Takeuchi, H. Chiba, A. Ito, H. Yoshioka, A. Kubota, T. Takahashi, and H. Nii, "43 Gb/s full-rate-clock 16 : 1 multiplexer and 1 : 16 demultiplexer with SFI-5 interface in SiGe BiCMOS technology," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2003, pp. 232–233.

[9] D. K. Shaeffer, H. Tao, Q. Lee, A. Ong, V. Condito, S. Benyamin, W. Wong, X. Si, S. Kudszus, and M. Tarsia, "A 40/43 Gb/s SONET OC-768 SiGe 4 : 1 MUX/CMU," in *Int. Solid-State Circuits Conf. Tech. Dig.*, 2003, pp. 236–237.

[10] K. Sano, K. Murata, S. Sugitani, H. Sugahara, and T. Enoki, "50-Gbit/s 4-bit multiplexer/demultiplexer chip-set using InP HEMTs," in *GaAs Int. Circuits Symp. Tech. Dig.*, 2002, pp. 207–210.

[11] H. Kano, T. Suzuki, S. Yamamura, Y. Nakasha, K. Sawada, T. Takahashi, K. Makiyama, T. Hirise, and Y. Watanabe, "A 50-Gbit/s 1 : 4 demultiplexer IC in InP-based HEMT technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 2002, pp. 75–78.

[12] M. Ida, K. Kurishima, H. Nakajima, N. Watanabe, and S. Yamahata, "Undoped-emitter InP/InGaAs HBT's for high-speed and low-power applications," in *Int. Electron Device Meeting Tech. Dig.*, 2000, pp. 854–856.

[13] K. Ishii, K. Murata, M. Ida, K. Kurishima, T. Enoki, T. Shibata, and E. Sano, "Very-high-speed selector IC using InP/InGaAs heterojunction bipolar transistors," *Electron. Lett.*, vol. 38, pp. 480–481, 2002.

[14] N. Ishihara, S. Fujita, M. Togashi, S. Hino, Y. Arai, N. Tanaka, Y. Kobayashi, and Y. Akazawa, "3.5-Gb/s × 4-ch Si bipolar LSI's for optical interconnections," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1493–1501, Dec. 1995.

[15] M. Yoneyama, A. Sano, K. Hagimoto, T. Otsuji, K. Murata, Y. Imai, S. Yamaguchi, T. Enoki, and E. Sano, "Optical repeater circuit design based on InAlAs/InGaAs HEMT digital IC technology," in *IEEE MTT-S Int. Microwave Symp. Dig.*, 1997, pp. 2274–2282.

Kiyoshi Ishii was born in Tokyo, Japan, on June 15, 1961. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Shinshu University, Nagano, Japan, in 1984, 1986, and 2001, respectively.

In 1986, he joined the Nippon Telegraph and Telephone (NTT) Corporation, Atsugi, Kanagawa, Japan, where he began researching electron beam lithography. Since 1990, he has been engaged in the research and development of high-speed ICs using Si-bipolar- and InP-based HBTs.

Dr. Ishii is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan, and the Japan Society of Applied Physics.

Hideyuki Nosaka (M'97) was born in Kanagawa, Japan, on March 4, 1971. He received the B.S. and M.S. degrees in physics from Keio University, Yokohama, Japan, in 1993 and 1995, respectively, and the Dr.Eng. degree in electronic and electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 2003, respectively.

In 1995, he joined the Nippon Telegraph and Telephone (NTT) Wireless Systems Laboratories, Yokosuka, Japan, where he was engaged in the research and development of monolithic microwave integrated circuits (MMICs) and frequency synthesizers. Since 1999, he has been engaged in research and development of 10- and 40-Gbit/s ICs for optical communication systems at NTT Photonics Laboratories, Atsugi, Kanagawa, Japan.

Dr. Nosaka is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He was the recipient of the 2001 Young Engineer Award presented by the IEICE.

Minoru Ida (M'95) was born on July 18, 1966, in Tokyo, Japan. He received the B.S. and M.S. degrees in electrical engineering from Keio University, Kanagawa, Japan, in 1989 and 1991, respectively.

In 1991, he joined the Nippon Telegraph and Telephone (NTT) LSI Laboratories, Kanagawa, Japan, where he was engaged in research on MOVPE growth and InP-based HBTs. From 1996 to 1998, he was with NTT Wireless Systems Laboratories, Kanagawa, Japan, where he was involved with GaAs MMICs for wireless applications. He is currently with the NTT Photonics Laboratories, Atsugi, Kanagawa, Japan, where he is involved in the research of ultrahigh-speed InP-based HBT devices and the development of the fabrication processes of ICs for optical networks.

Kenji Kurishima received the B.S., M.S., and Ph.D. degrees from the Tokyo Institute of Technology, Tokyo, Japan, in 1987, 1989, and 1997, respectively.

In 1989, he joined the Nippon Telegraph and Telephone (NTT) Electrical Communications Laboratories, Atsugi, Kanagawa, Japan, where he is currently engaged in research on InP-based HBTs and MOVPE growth. His current research interests include the design and fabrication of high-speed electronic devices for future communications systems.

Shoji Yamahata received the B.S. and M.S. degrees in polymer science and Ph.D. degree in physics from Hokkaido University, Hokkaido, Japan, in 1982, 1984, and 1996, respectively.

In 1984, he joined the Nippon Telegraph and Telephone (NTT) Electrical Communications Laboratories, Kanagawa, Japan, where he was involved with ion-implantations for III–V compound semiconductors. Since 1989, he has been engaged in research on GaAs- and InP-based HBTs with NTT Photonics Laboratories, Atsugi, Kanagawa, Japan. He current research interests include high-frequency characteristics of devices and their fabrication technique.

Dr. Yamahata is a member of the Japan Society of Applied Physics.

Takatomo Enoki (M'91–SM'01) was born in Tottori, Japan, in 1959. He received the B.S. and M.S. degrees in physics and Dr.Eng. degree in electronic and electrical engineering from the Tokyo Institute of Technology, Tokyo, Japan, in 1982, 1984, and 1996, respectively.

In 1984, he joined the Atsugi Electrical Communications Laboratories, the Nippon Telegraph and Telephone (NTT), Kanagawa, Japan. Since then, he has been engaged in research and development on fabrication technologies for high-frequency and high-speed GaAs MESFETs and ICs. Since 1989, he has studied and developed ultrahigh-speed and low-noise heterostructure field-effect transistors (FETs) and their ICs on an InP substrate. From 1997 to 1999, he was a Senior Manager in the Research Planning Division, where he had focused on research and development of ultrahigh-speed heterostructure ICs for optical communications systems with NTT Photonics Laboratories. He is currently a Senior Research Engineer, Supervisor, and a Research-Group Leader in charge of research and development of advanced heterostructure electron devices for future communications.

Dr. Enoki is a chairman of the Electron Device Technical Group of the Institute of Electronics, Information, and Communication Engineers (IEICE), Japan. He is a member of the Japan Society of Applied Physics (JSAP), the Institute of Electrical Engineering of Japan (IEEJ), and the Optical Society of America (OSA).

Tsugumichi Shibata (M'87–SM'01) graduated from the Tokyo National College of Technology, Tokyo, Japan, in 1980, and received the B.S., M.S., and Ph.D. degrees in electrical engineering from the University of Tokyo, Tokyo, Japan, in 1983, 1985, and 1995, respectively.

In 1985, he joined the Atsugi Electrical Communications Laboratories, Nippon Telegraph and Telephone (NTT) Corporation, where he was engaged in research on electromagnetic-field analyses, electrooptic sampling of subpicosecond signals in ICs, and the design of high-speed devices and circuits for data transmission systems. From 1996 to 1997, he was a Visiting Scholar with the University of California at Los Angeles (UCLA), where he performed research on diakoptics in numerical field simulation. He is currently a Senior Research Engineer and Supervisor with the NTT Photonics Laboratories, Atsugi, Kanagawa, Japan, where he oversees a research group involved with high-speed circuit design.

Dr. Shibata is a member of the Institute of Electronics, Information and Communication Engineers (IEICE), Japan. He has served as a member of the Technical Program Committee (TPC) of the IEEE Microwave Theory and Techniques Society (IEEE MTT-S) International Microwave Symposium (IMS) since 1999. He was a member of the Paper Review Board of the 1998 and 2002 Asia–Pacific Microwave Conferences (APMCs).

Eiichi Sano (M'84), photograph and biography not available at time of publication.